gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in the other inverter;

coupling a bit line to [a] another gate of the dual-gate transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

REMARKS

Applicant has reviewed and considered the Office Action mailed on July 18, 2001, and the references cited therewith.

Claims 10, 11, 23, 29, 32, and 37 are amended, claims 1, 2, 4, 6-9 are canceled; as a result, claims 10, 11, 13-18, 20-24, 26-38, and 40-45 are now pending in this application. The claims are amended to clarify the claimed invention.

Applicant respectfully requests reconsideration and allowance of all claims pending in the application in view of the amendments above and the remarks that follow.

§112 Rejection of the Claims

Claims 1, 2, 17, 18, 20-24 and 26-45 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has elected to cancel claim 1-9 solely for the purpose of expediting the patent application process in a manner consistent with the PTO's Patent Business Goals (PBG) 65 Fed. Reg. 54603 (September 8, 2000). Claims 10, 11, 23, 29, 32, and 37 have been amended to more clearly define Applicant's invention. In particular, the claims have been amended to reflect the Applicant's novel use of a dual-gated MOSFET, as taught on page 10, lines 16-30. No new matter has been introduced. Based on the discussion above regarding Applicant's definition of a dual-gated MOSFET, it is submitted that claims 17, 23, 29, 32, 37, 40, 44 and 45 are descriptive of Applicant's invention and render the claims definite. Applicant respectfully requests that rejections of claims 17, 18, 20-24 and 26-45 under 35 USC § 112 be withdrawn.

§102 Rejection of the Claims

Claims 1, 2, 4, 6, 7, 10, 11, 13, 14, 17, 18, 20, 23, 24, 29, 33-38, 44 and 45 were rejected under 35 USC § 102(e) as being anticipated by Austin (U.S. 5,982,690).

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

All pending claims in the application cite including a pair of dual-gated metal oxide semiconductors in each amplifier (claim 10, 11,and 13-16), and each inverter (claim17, 18, 20-24, 26-38, and 40-45). In contrast, Austin cites in Fig. 1D and col.5 lines 7-10, " third and fourth parallel connected (PC) transistor pairs 153 and 154." Using two transistors in a circuit as one pair of parallel connected transistors is significantly different than using a single dual-gated MOSFET. Nowhere does Austin include, teach or suggest the use of a dual-gated transistor in a latch, amplifier, or sense amplifier.

Because Austin does not include within its corners all elements of Applicant's invention, a 35 U.S.C. §102(e) rejection is no longer appropriate. Applicant respectfully contends that the independent claims as amended and all claims depending therefrom are in condition for allowance. Therefore, Applicant respectfully requests withdrawal of Examiner's §102(e) rejection as to claims 10, 11, 13, 14, 17, 18, 20, 23, 24, 29, 33-38, 44 and 45.

§103 Rejection of the Claims

Claims 8, 9, 15, 16, 21, 22, 26, 27 and 30-32 were rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. 5,982,690) .

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

As to claims 15, 16, 21, 22, 26, 27, and 30-32, these claims cite using a dual-gated metal oxide semiconductor. In contrast, Austin in Fig. 1D and col.5 lines 7-10 cites " third and fourth parallel connected (PC) transistor pairs 153 and 154." Nowhere does Austin disclose, teach or suggest the use of a dual-gated transistor in a latch, amplifier, or sense amplifier. The teaching or

suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02. Since Austin does not disclose, teach, or suggest every element of these claims, claims 15, 16, 21, 22, 26, 27, and 30-32 are patentable over Austin. Applicant respectfully requests withdrawal of Examiner's §103(a) rejection as to claims 15, 16, 21, 22, 26, 27, and 30-32.

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al (US 6,069,828) in view of Austin (U.S. 5,982,690).

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

As to claims 28 and 40-43, these claims cite using a dual-gated metal-oxide semiconductor. As mentioned above, Austin does not disclose, teach, or suggest the use of a dual-gated transistor. As to Kaneko et al., the Office Action states in reference to Kaneko et al. that "figure 2 shows all the elements of the claim except for the detail of the sense amplifier," indicating that Kaneko et al. nowhere discloses, teaches, or suggests a dual-gated transistor. Since neither Austin, Kaneko et al. or their combination disclose, teach, or suggest all the elements of these claims, claims 28 and 40-43 are patentable over Kaneko et al. in view of Austin. Applicant respectfully requests withdrawal of Examiner's §103(a) rejection as to claims 28 and 40-43.

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Conclusion

Applicant respectfully submits that the pending claims 10, 11, 13-18, 20-24, 26-38, and 40-45 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 10/10/2001 By _____
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Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 10th day of October, 2001.

Amy Moriarty _____
Name Signature

CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES
Applicant: Leonard Forbes et al.
Serial No.: 09/320,421

The paragraph beginning at page 10, line 16:

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In an alternative embodiment, the pair of transistors, M3, M5, and M4, M6, in each inverter, B1 and B2, comprise a dual-gated metal oxide semiconductor field effect transistor (MOSFET), 298 and 299, respectively, in each inverter, B1 and B2. In this embodiment, each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET in each inverter, B1 and B2. In this embodiment, the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and the dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors, each driven by one of the dual gates. In this embodiment, the drain regions, 204 and 212, for one of the cross-coupled inverters, B1, is further coupled to a gate of the transistor of the first conductivity type, M2, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2. Similarly, the drain regions, 206 and 214, for inverter, B2, is coupled to a gate of the transistor of the first conductivity type, M1, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2.

Docket No. 303.580US1
WD # 320804

Micron Ref. No. 98-0588

Clean Version of Pending Claims

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES
Applicant: Leonard Forbes et al.
Serial No.: 09/320,421

Claims 10, 11, 13-18, 20-24, 26-38 and 40-45, as of October 10, 2001 (response to first office action after CPA filed).

10. (Thrice Amended) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein a drain region for the dual-gated MOSFET is coupled to a drain region of the first transistor in the same amplifier, is coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier in the pair of cross-coupled amplifiers, and is coupled to a gate of the dual-gated MOSFET in the other amplifier in the pair of cross-coupled amplifiers;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the dual-gated MOSFET.

11. (Thrice Amended) The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET include n-channel metal oxide semiconductor (NMOS) transistors.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

17. (Once Amended) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines

is coupled to another gate of the dual-gated MOSFET in each inverter respectively; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. (Thrice Amended) A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region of for the

cont C3

dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. (Thrice Amended) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. (Thrice Amended) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to another gate of the dual-gate transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes directly coupling the drain region for the transistor of the first conductivity type and the drain region for the dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to one gate of the dual-gate transistor in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the dual-gate transistor of a second conductivity type as an n-channel metal oxide semiconductor (NMOS) transistor.

35. The method of claim 33, wherein the method further includes coupling a bit line to another gate of the dual-gate transistor in each inverter.

36. The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter. .

37. (Thrice Amended) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a dual-gate transistor of a second conductivity type, wherein forming the dual-gate transistor includes coupling the drain region for the dual-gate transistor to a drain region of the first transistor in each inverter, directly coupling the drain region for the dual-gate transistor in each inverter to a gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in the other inverter;

coupling a bit line to another gate of the dual-gate transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the dual-gate transistor of a second conductivity type includes forming an n-channel metal oxide semiconductor (NMOS) transistor.

40. A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a dual-gate transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter directly to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a dual-gate transistor in the first inverter.

41. The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. A method for operating a sense amplifier, comprising:

providing a first bit line signal to a first gate of a dual-gate transistor in a first inverter of the sense amplifier;

providing a second bit line signal to a first gate of a dual-gate transistor in a second inverter of the sense amplifier

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a first gate of a dual-gate transistor in a first inverter of the sense amplifier

wherein providing the input signal from the bit line to the first gate of the dual-gate transistor in the first inverter of the sense amplifier drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a dual-gate transistor in a

second inverter; and

wherein providing the input signal to the first gate of the dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.